

- 1.(currently amended) An apparatus comprising:

 a processor, coupled to a cache memory;

 the cache memory with a plurality of cache lines, each cache line with at least one status bit to represent whether the cache line contains a defect and at least one valid bit to indicate whether the line is valid; and

 a logic to perform at least one test of the plurality of cache lines and to set the status bit for at least one of the plurality of cache lines.
- 2.(original) The apparatus of claim 1 wherein the logic is a programmable built in self-test (PBIST) logic.
- 3.(original) The apparatus of claim 1 wherein the logic is a plurality of scan chains and a test access port to accept automatic test pattern generation (ATPG) patterns.
- 4.(original) The apparatus of claim 1 wherein the status bit is stored in a six-transistor static random access memory cell.
- 5.(original) The apparatus of claim 1 wherein the status bit is stored in a register file cell.
- 6.(original) The apparatus of claim 1 wherein the status bit is stored in a fuse.
- 7.(original) The apparatus of claim 1 wherein the status bit is a read only bit during normal operation of the system.

8.(original) The apparatus of claim 1 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache.

9.(original) The apparatus of claim 2 wherein the PBIST logic can set the status bit during initialization of the cache memory.

10. (currently amended) An article comprising:

a storage medium having stored thereon instructions, that, when executed by a computing platform, result in execution of testing a processor's cache memory with a plurality of cache lines;

generating a test pattern;

stimulating the cache memory with the test pattern; [and]

writing to at least one status bit for each cache line to indicate whether the cache line contains a defect; and

reading at least one valid bit to indicate whether the cache line is valid.

11.(original) The article of claim 10 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache.

12.(original) The article of claim 10 wherein the status bit is stored in either one of a six-transistor static random access memory cell, a register file cell, or a fuse.

13.(original) The article of claim 10 wherein the status bit is a read only bit during normal operation of the cache memory.

14.(currently amended) A method of configuring a cache memory with a plurality of cache lines comprising:

testing the plurality of cache lines;

setting a status bit for at least one cache line to indicate whether the cache line has a defect as a result of the testing; and

the status bit is a read only bit during normal operation of the cache memory. [disabling the cache lines when the status bit indicates the defect].

15.(original) The method of claim 14 wherein the setting a status bit comprises storing the bit in either one of a six-transistor static random access memory cell, a register file cell, or a fuse.

16.(original) The method of claim 14 wherein the status bit is stored in either one of a six-transistor static random access memory cell, a register file cell, or a fuse.

17.(currently deleted) [The method of claim 14 wherein the status bit is a read only bit during normal operation of the cache memory].